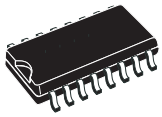
L6591

PWM controller for ZVS half-bridge

Features

- Complementary PWM control for soft-switched half-bridge with programmable dead-time
- Up to 500 kHz operating frequency
- On-board high-voltage start-up
- Advanced light load management
- Adaptive UVLO
- Pulse-by-pulse OCP
- OLP (latched or autorestart)
- Transformer saturation detection
- Interface with PFC controller
- Latched disable input
- Input for power-on sequencing or brownout protection
- Programmable soft-start
- 4 % precision external reference



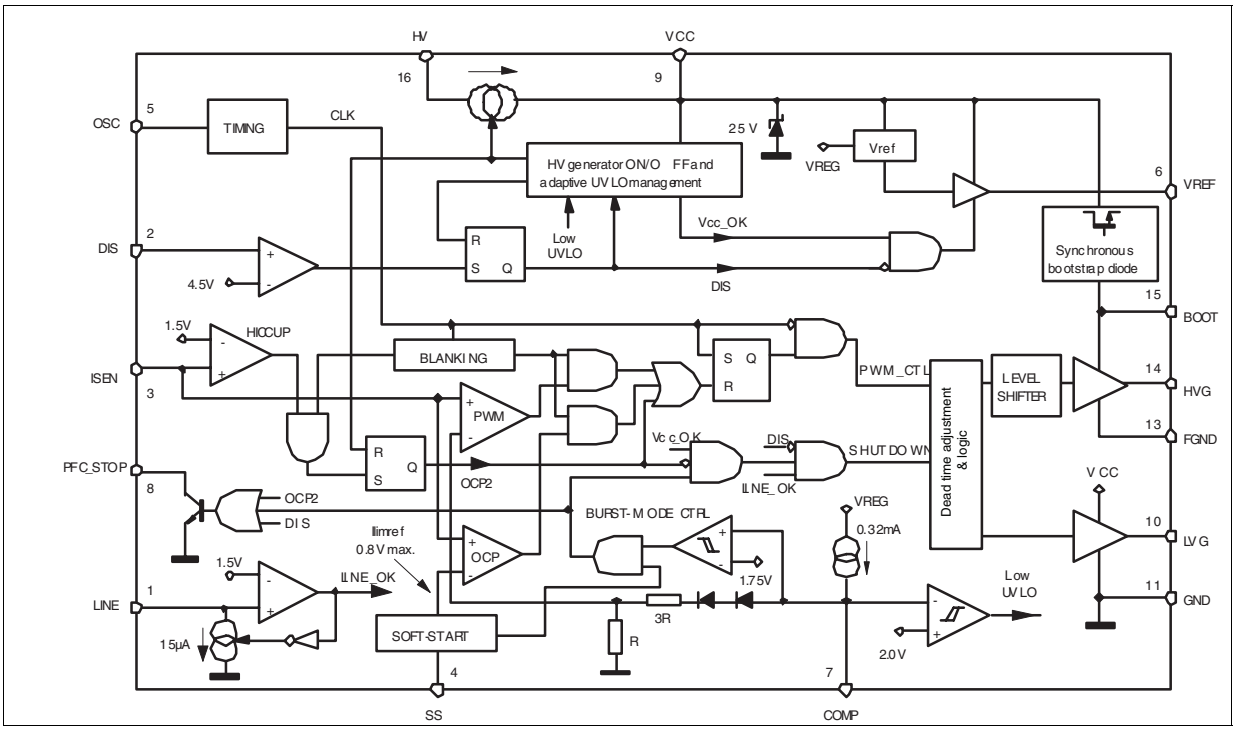
SO16 narrow

- 600 V-rail compatible high-side gate driver with integrated bootstrap diode and high dV/dt immunity
- SO16N package

Applications

- High power AC-DC adapter/charger
- Desktop PC, entry-level server
- Telecom SMPS

Figure 1. Typical application circuit



Contents

1 Device description

The L6591 is a double-ended PWM controller specific for the soft-switched half-bridge topology. It provides complementary PWM control, where the high-side switch is driven ON for a duty cycle D and the low-side switch for a duty cycle 1-D, with D 50 %. An externally programmable dead-time inserted between the turn-off of one switch and the turn-on of the other one guarantees soft-switching and enables high-frequency operation.

To drive the high-side switch with the bootstrap approach, the IC incorporates a high-voltage floating structure able to withstand more than 600 V with a synchronous-driven high-voltage DMOS that replaces the external fast-recovery bootstrap diode.

The IC enables the designer to set the operating frequency of the converter by means of an externally programmable oscillator: the maximum duty cycle is digitally clipped at 50 % by a T-flip-flop, so that the operating frequency will be half that of the oscillator.

At very light load the IC enters a controlled burst-mode operation that, along with the built-in non-dissipative high-voltage start-up circuit and the low quiescent current, helps keep low the consumption from the mains and be compliant with energy saving recommendations.

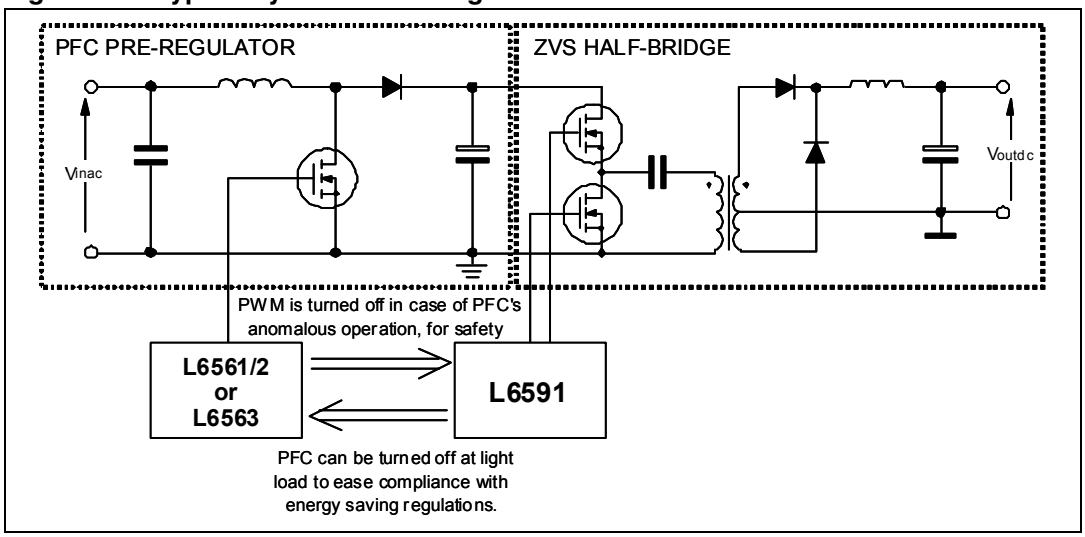
To allow compliance with these standards in two-stage power-factor-corrected systems as well, an interface with the PFC controller is provided that enables to switch off the pre-regulator between one burst and the following one.

An innovative adaptive UVLO helps minimize the issues related to the fluctuations of the self-supply voltage with the output load, due to transformer's parasitic.

IC's protection functions include: not-latched input undervoltage (brownout), a first-level OCP with delayed shutdown able to protect the system during overload and short circuit conditions (either auto-restart or latch mode can be selected) and a second-level OCP that latches off the IC when the transformer saturates or one of the secondary diodes fails short. Finally, a latched disable function allows easy implementation of OTP or OVP.

Programmable soft-start and digital leading-edge blanking on current sense input pin complete the equipment of the IC.

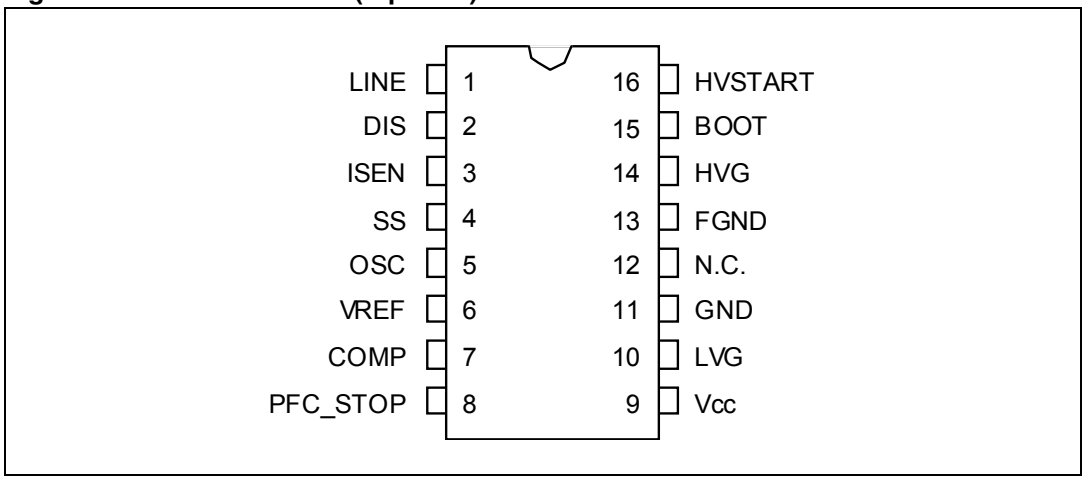
Figure 2. Typical system block diagram



2 Pin settings

2.1 Connection

Figure 3. Pin connection (top view)



2.2 Functions

Table 1. Pin functions

Pin N.	Name	Function
1	LINE	Line sensing input. The pin is to be connected to the high-voltage input bus with a resistor divider. A voltage below 1.25 V shuts down the IC, lowers its consumption and discharges the soft-start capacitor. IC's operation is re-enabled as the voltage exceeds 1.25 V. The comparator is provided with current hysteresis: an internal 15 µA current generator is ON as long as the voltage applied at the pin is below 1.25 V and is OFF if this value is exceeded. Bypass the pin with a capacitor to GND (#11) to reduce noise pick-up. The pin is intended for either power-on sequencing in systems with PFC, or brownout protection. Tie to Vcc (#9) with a 220 to 330 kW resistor if the function is not used.
2	DIS	Latched device shutdown. Internally the pin connects a comparator that, when the voltage on the pin exceeds 4.5 V, shuts the IC down and brings its consumption to a value barely higher than before start-up. The information is latched and it is necessary to recycle the input power to restart the IC: the latch is removed as the voltage on the Vcc pin (#9) goes below the UVLO threshold. Connect the pin to GND (#11) if the function is not used.

Table 1. Pin functions (continued)

Pin N.	Name	Function
3	ISEN	Current sense (PWM comparator) input. The voltage on this pin is internally compared with an internal reference derived from the voltage on pin COMP and when they are equal the high-side gate drive output (previously asserted high by the clock signal generated by the oscillator) is driven low to turn off the upper power MOSFET; the lower MOSFET is turned on after a delay programmed by the timing capacitor at pin OSC (#5). The pin is equipped with 200 ns blanking time for improved noise immunity. A second comparator referenced at 0.8 V turns off the upper MOSFET if the voltage at the pin exceeds the threshold, overriding the PWM comparator (pulse-by-pulse OCP). A third comparison level located at 1.5 V shuts the device down and brings its consumption almost to a “before start-up” level (hiccup-mode OCP) to prevent uncontrolled current rise. A logic circuit improves sensitivity to temporary disturbances.
4	SS	Soft-start. An internal 20 µA generator charges an external capacitor connected between the pin and GND (#11) generating a voltage ramp. During the ramp, the internal reference for pulse-by-pulse OCP (see pin #3, ISEN) rises linearly starting from zero to its final value, thus causing the duty cycle of the upper MOSFET to rise starting from zero as well, and all the functions monitoring pin COMP (#7) are disabled. The same capacitor is used to delay IC’s shutdown (latch-off or auto-restart mode selectable) after detecting an overcurrent condition. The SS capacitor is quickly discharged as the chip goes into UVLO.
5	OSC	Oscillator pin. A resistor to VREF (#6) and a capacitor from the pin to GND (#11) define the oscillator frequency. The maximum duty cycle is limited below 50 % by an internal T-flip-flop. As a result, the switching frequency will be half that of the oscillator. The capacitor value defines the dead-time separating the conduction state of either MOSFET. This capacitor should not be lower than 220 pF.
6	VREF	Voltage reference. An internal generator furnishes an accurate voltage reference (5 V±4 %, all inclusive) that can be used to supply up to 5 mA to an external circuit. A small film capacitor (0.1 µF typ.), connected between this pin and GND (#11) is recommended to ensure the stability of the generator and to prevent noise from affecting the reference.
7	COMP	Control input for PWM regulation. The pin is to be driven by the phototransistor (emitter-grounded) of an octocoupler to modulate the voltage by modulating the current sunk from (sourced by) the pin (0.4 mA typ.). It is recommended to place a small filter capacitor between the pin and GND (#11), as close to the IC as possible to reduce switching noise pick up, to set a pole in the output-to-control transfer function. A voltage lower than 1.75 V shuts down the IC and reduces its current consumption. The chip restarts as the voltage exceeds 1.8 V. This function realizes burst-mode operation at light load.
8	PFC_STOP	Open-drain ON/OFF control of PFC controller. This pin is intended for temporarily stopping the PFC controller at light load in systems comprising a PFC pre-regulator, during burst-mode operation (see pin COMP, #7). The pin, normally open, goes low if the voltage on COMP is lower than 1.75 V and opens when the voltage on pin COMP exceeds 1.8V. Whenever the IC is shut down (SS > 5 V, DIS>4.5, ISEN >1.5 V) the pin is low as well, provided the supply voltage of the IC is above the restart threshold (typ. 5 V). It is open during UVLO. Leave the pin open if not used

Table 1. Pin functions (continued)

Pin N.	Name	Function
9	Vcc	Supply voltage of both the signal part of the IC and the low-side gate driver. The internal high voltage generator charges an electrolytic capacitor connected between this pin and GND (#11) as long as the voltage on the pin is below the start-up threshold of the IC, after that it is disabled and the chip turns on. Sometimes a small bypass capacitor (0.1 µF typ.) to GND might be useful to get a clean bias voltage for the signal part of the IC. The minimum operating voltage (UVLO) is adapted to the loading conditions of the converter to ease burst-mode operation, during which the available supply voltage for the IC drops.
10	LVG	Low-side gate-drive output. The driver is capable of 0.3 A min. source and 0.8A min. sink peak current to drive the gate of the lower MOSFET of the half-bridge leg. The pin is actively pulled to GND (#11) during UVLO.
11	GND	Chip ground. Current return for both the low-side gate-drive current and the bias current of the IC. All of the ground connections of the bias components should be tied to a track going to this pin and kept separate from any pulsed current return.
12	N.C.	High-voltage spacer. The pin is not connected internally to isolate the group of high-voltage pins and comply with safety regulations (creepage distance) on the PCB.
13	FGND	High-side gate-drive floating ground. Current return for the high-side gate-drive current. Layout carefully the connection of this pin to avoid too large spikes below ground.
14	HVG	High-side floating gate-drive output. The driver is capable of 0.3 A min. source and 0.8 A min. sink peak current to drive the gate of the upper MOSFET of the half-bridge leg. A pull-down resistor between this pin and pin 13 (FGND) makes sure that the gate is never floating during UVLO.
15	BOOT	High-side gate-drive floating supply voltage. The bootstrap capacitor connected between this pin and pin 13 (FGND) is fed by an internal synchronous bootstrap diode driven in-phase with the low-side gate-drive. This patented structure can replace the normally used external diode.
16	HVSTART	High-voltage start-up. The pin is to be connected directly to the rectified mains voltage. A 0.8 mA internal current source charges the capacitor connected between pin Vcc (#9) and GND (#11) until the voltage on the Vcc pin reaches the start-up threshold. Normally it is re-enabled when the voltage on the Vcc pin falls below 5 V, except under latched shutdown conditions, in which case it is re-enabled as the Vcc voltage falls 1 V below the start-up threshold to keep the latch active.

3 Electrical data

3.1 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
$V_{HVSTART}$	16	Voltage range (referred to ground)	-0.3 to 700	V
I_{HVS}	16	Input current	Self-limited	A
V_{BOOT}	15	Floating supply voltage	-1 to 618	V
V_{FGND}	13	Floating ground voltage	-3 to V_{BOOT} -18	V
dV_{FGND}/dt	13	Floating ground slew rate	50	V/ns
V_{CC}	9	IC supply voltage (Icc = 20 mA)	Self-limited	V
I_{HVG}, I_{LVG}	10, 14	Gate-drives peak current	Self-limited	A
I_{PFC_STOP}	8	Max. sink current (V_{PFC_STOP} = 25 V)	Self-limited	A
$V_{LINEmax}$	1	Maximum pin voltage (Ipin ≤ 1 mA)	Self-limited	V
---	2 to 7	Analog inputs and outputs	-0.3 to 7	V
ISEN	3	Current sense input	-3 to 7	V
P_{TOT}		Power dissipation @ T_A = 50 °C	0.75	W
T_J		Junction temperature operating range	-40 to 150	°C
T_{STG}		Storage temperature	-55 to 150	°C

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient (1)	120	°C/W

1. Value depending on PCB copper area and thickness.

4 Electrical characteristics

Table 4. Electrical characteristics
(T_J = 0 to 105 °C, Vcc = 15 V, V_{BOOT} = 12 V, C_{HVG} = C_{LVG} = 1 nF; R_T = 22 kΩ, C_T = 330 pF; unless otherwise specified)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
IC supply voltage						
Vcc	Operating range after turn-on	$V_{COMP} > V_{COMPL}$	11.3		22	V
		$V_{COMP} = V_{COMPL}$	9.2		22	
Vcc_{On}	Turn-on threshold	(1)	13	14	15	V
Vcc_{Off}	Turn-off threshold	(1) $V_{COMP} > V_{COMPL}$	9.7	10.5	11.3	V
		(1) $V_{COMP} = V_{COMPL}$	8.2	8.7	9.2	
Hys	Hysteresis	$V_{COMP} > V_{COMPL}$	3.0	3.5		V
V_Z	Vcc clamp voltage	Icc = 15 mA	22	25	28	V
Supply current						
$I_{start-up}$	Start-up current	Before turn-on, Vcc = 12.5 V		190	250	µA
Iq	Quiescent current	After turn-on		2.8	3.5	mA
Icc	Operating supply current			5.3	8	mA
Iq_{dis}	Shutdown quiescent current	V_{DIS} > 4.5 V, V_{ISEN} > 1.5 V			0.35	mA
		V_{COMP} = 1.64 V			2.2	mA
		V_{LINE} < 1.44 V			0.35	mA
High-side floating gate-drive supply						
V_{BOOT}	Operating supply voltage	Referred to FGND pin			17	V
I_{qBOOT}	Quiescent current	V_{FGND} = 0		500	800	µA
I_{LK}	High-voltage leakage	V_{FGND} = V_{BOOT} = V_{HVG} = 600 V			10	µA
$R_{DS(on)}$	Synchronous bootstrap diode on-resistance	V_{LVG} = HIGH		125		Ω
High-voltage start-up generator						
V_{HV}	Breakdown voltage	I_{HV} < 100 µA	700			V
$V_{HVstart}$	Start voltage	I_{Vcc} < 100 µA	60	75	90	V
I_{charge}	Vcc charge current	$V_{HV} > V_{Hvstart}$, Vcc> 3V	0.55	0.75	1	mA
$I_{HV, ON}$	ON-state current	$V_{HV} > V_{Hvstart}$, Vcc> 3 V			1.6	mA
		$V_{HV} > V_{Hvstart}$, Vcc = 0			0.8	
$I_{HV, OFF}$	Leakage current (OFF-state)	V_{HV} = 400 V			40	µA

Table 4. Electrical characteristics (continued)
(T_J = 0 to 105 °C, Vcc = 15 V, V_{BOOT} = 12 V, C_{HVG} = C_{LVG} = 1 nF; R_T = 22 kΩ, C_T = 330 pF; unless otherwise specified)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
$V_{CCrestart}$	HV generator restart voltage	(1)	4.4	5	5.6	V
		(1) After DIS tripping	12.2	13.2	14.2	V
Reference voltage						
V_{REF}	Output voltage	(2) T_J = 25 °C; I_{REF} = 1 mA	4.9	5	5.1	V
V_{REF}	Total variation	Vcc= 9.2 to 22 V, I_{REF} = 1 to 5 mA	4.8		5.2	V
I_{REF}	Short circuit current	V_{REF} = 0	10		30	mA
	Sink capability in UVLO	Vcc = 6 V; Isink = 0.5 mA		0.2	0.5	V
Current sense comparator						
I_{ISEN}	Input bias current	V_{ISEN} = 0			-1	µA
t_{LEB}	Leading edge blanking	After V_{HVG} low-to-high transition		200		ns
$t_{d(H-L)}$	Delay to output				170	ns
	Gain		3.8	4	4.2	V/V
V_{ISENx}	Maximum signal	(2) V_{COMP} = 5 V	0.76	0.8	0.84	V
$V_{ISENdis}$	Hiccup-mode OCP level	(2)	1.4	1.5	1.65	V
PWM control and burst-mode control						
V_{COMPH}	Maximum level	I_{COMP} = 0	5.5			V
I_{COMP}	Source current	V_{COMP} = 2 V	240	320	400	µA
R_{COMP}	Dynamic resistance	V_{COMP} = 2 to 4 V		25		kΩ
$V_{COMPBon}$	Burst-mode on threshold	(2) V_{COMP} falling	1.68	1.75	1.82	V
Hys	Burst-mode hysteresis	V_{COMP} rising		70		mV
D_{max}	Maximum duty cycle	V_{COMP} = 5 V	45		50	%
Adaptive UVLO						
V_{COMPL}	UVLO shift threshold	(2)	1.9	2	2.1	V
Line sensing						
Vth	Threshold voltage	Voltage rising or falling	1.22	1.25	1.28	V
I_{Hys}	Current hysteresis	Vcc > 5 V	13.2	14.7	16.2	µA
V_{clamp}	Clamp level	I_{LINE} = 1 mA	2.8	3		V

Table 4. Electrical characteristics (continued)
(T_J = 0 to 105 °C, Vcc = 15 V, V_{BOOT} = 12 V, C_{HVG} = C_{LVG} = 1 nF; R_T = 22 kΩ, C_T = 330 pF; unless otherwise specified)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
DIS function						
I_{OTP}	Input bias current	V_{DIS} = 0 to Vth			-1	µA
Vth	Disable threshold		4.275	4.5	4.725	V
Oscillator and dead-time programming						
f_{osc}	Oscillation frequency	T_J = 25 °C	170	180	190	kHz
		Vcc = 9.2 to 22 V	168	180	192	kHz
Vpk	Oscillator peak voltage	(2)	2.85	3	3.15	V
Vvy	Oscillator valley voltage	(2)	0.75	0.9	1.05	V
T_{dead}	Dead-time (V_{HVG} high-to-low to V_{LVG} low-to-high transition)			0.42		µs
		C_T = 1 nF		1.0		
	Dead-time (V_{LVG} high-to-low to V_{HVG} low-to-high transition)			0.42		
		C_T = 1 nF		1.0		
Soft-start						
I_{SSC}	Charge current	T_J = 25 °C, V_{SS} < 1.5 V, V_{COMP} = 4 V	14	17	20	µA
		T_J = 25 °C, V_{SS} > 1.5 V, V_{COMP} = V_{COMPH}	3.0	4.2	5.4	
I_{Ssdis}	Discharge current	V_{SS} > 1.5 V	3.0	4.2	5.4	µA
$V_{Ssclamp}$	High saturation voltage	V_{COMP} = 4 V		2		V
V_{SSDIS}	Disable level	(2) V_{COMP} = V_{COMPH}	4.85	5	5.15	V
V_{SSLAT}	Latch-off level	V_{COMP} = V_{COMPH}		6.4		V
PFC_STOP function						
I_{leak}	High level leakage current	V_{PFC_STOP} = Vcc, V_{COMP} = 2 V			1	µA
V_L	Low saturation level	I_{PFC_STOP} = 2 mA V_{COMP} = 1.5 V			0.1	V
Low-side gate driver (voltages referred to GND)						
V_{LVGL}	Output low voltage	I_{sink} = 200 mA			1.0	V
V_{LVGH}	Output high voltage	I_{source} = 5 mA	12.8	13.3		V
$I_{sourcepk}$	Peak source current (3)		-0.3			A
I_{sinkpk}	Peak sink current (3)		0.8			A
t_f	Fall time			40		ns

Table 4. Electrical characteristics (continued)
(T_J = 0 to 105 °C, Vcc = 15 V, V_{BOOT} = 12 V, C_{HVG} = C_{LVG} = 1 nF; R_T = 22 kΩ, C_T = 330 pF; unless otherwise specified)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
t_r	Rise time			80		ns
	UVLO saturation	Vcc = 0 to Vcc_{On}, I_{sink} = 1 mA			1.1	V
High-side gate driver (voltages referred to FGND)						
V_{HVGL}	Output low voltage	I_{sink} = 200 mA			1.5	V
V_{HVGH}	Output high voltage	I_{source} = 5 mA	11	11.9		V
$I_{sourcepk}$	Peak source current (3)		-0.3			A
I_{sinkpk}	Peak sink current (3)		0.8			A
t_f	Fall time			40		ns
t_r	Rise time			80		ns
	Pull-down resistor			25		kΩ

1. Parameters in tracking each other
2. Parameters in tracking each other
3. Parameters guaranteed by design

5 Application information

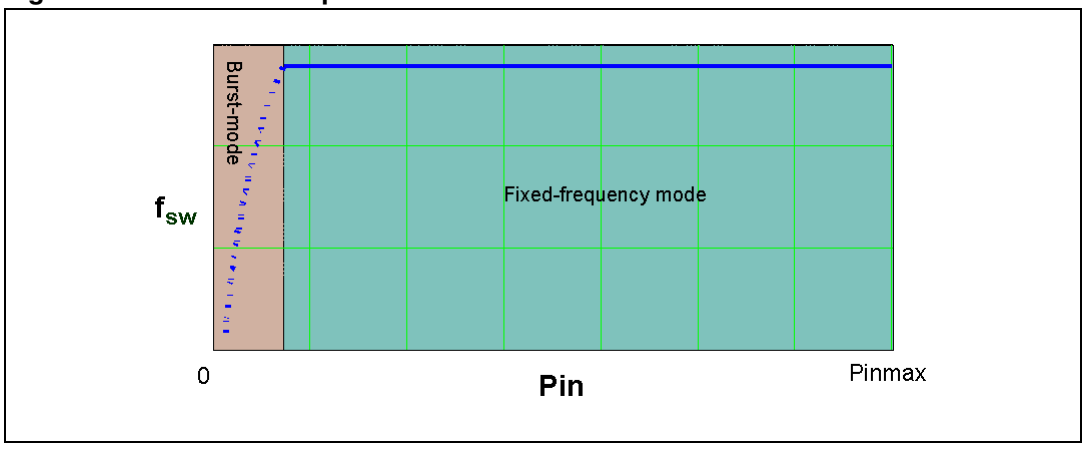
The L6591 is an advanced current-mode PWM controller specific for fixed-frequency, peak-current-mode-controlled ZVS half-bridge converters. In these converters the switches (MOSFET's) are controlled with complementary duty cycle: the high-side MOSFET is driven ON for a duty cycle D and the low-side MOSFET for a duty cycle 1-D. For a proper operation the maximum allowed duty cycle must be limited below 50 %.

An externally programmable dead-time T_D inserted between the turn-off of one MOSFET and the turn-on of the other one ensures soft-switching and enables high-frequency operation with high efficiency and low EMI emissions. See *Section 5.6: Oscillator and dead-time programming on page 19* section for more information on how to program T_D.

The device is able to operate in different modes (*Figure 4*), depending on the converter's load conditions:

1. Fixed frequency at heavy load. A relaxation oscillator, externally programmable with a capacitor and a resistor generates a sawtooth and releases clock pulses during the falling edges of the sawtooth. In this region the low-side MOSFET is turned off by the even pulses of the clock signal and the high-side MOSFET is turned on after a delay; the high-side MOSFET is turned off and, after a delay, the low-side MOSFET is turned on in response to the control loop.
2. Burst-mode control with no or very light load. When the load is extremely light or disconnected, the converter will enter a controlled on/off operation with fixed duty cycle, where a series of few switching cycles are spaced out by long periods where both MOSFET's are in OFF-state. A load decrease will be then translated into a frequency reduction, which can go down even to few hundred hertz, thus minimizing all frequency-related losses and making it easier to comply with energy saving regulations. Being the peak current very low, no issue of audible noise arises.

Figure 4. Multi-mode operation



5.1 High-voltage start-up generator

Figure 5 shows the internal schematic of the high-voltage start-up generator (HV generator). It is made up of a high-voltage N-channel FET, whose gate is biased by a 15 MW resistor, with a temperature-compensated current generator connected to its source.

With reference to the timing diagram of *Figure 6*, when power is first applied to the converter the voltage on the bulk capacitor (Vin) builds up and, as it reaches about 80 V, the HV generator is enabled to operate (HV_EN is pulled high) and draws about 1 mA. This current, diminished by the IC consumption, charges the bypass capacitor connected between pin Vcc (9) and ground and makes its voltage rise almost linearly.

As the Vcc voltage reaches the start-up threshold (13.5 V typ.) the IC starts operating and the HV generator is cut off by the Vcc_OK signal asserted high. The IC is powered by the energy stored in the Vcc capacitor until the self-supply circuit develops a voltage high enough to sustain the operation. The residual consumption of this circuit is just the one on the 15 MW resistor (≈10 mW at 400 Vdc), typically 50-70 times lower, under the same conditions, as compared to a standard start-up circuit made with an external dropping resistor.

Figure 5. High-voltage start-up generator: internal schematic

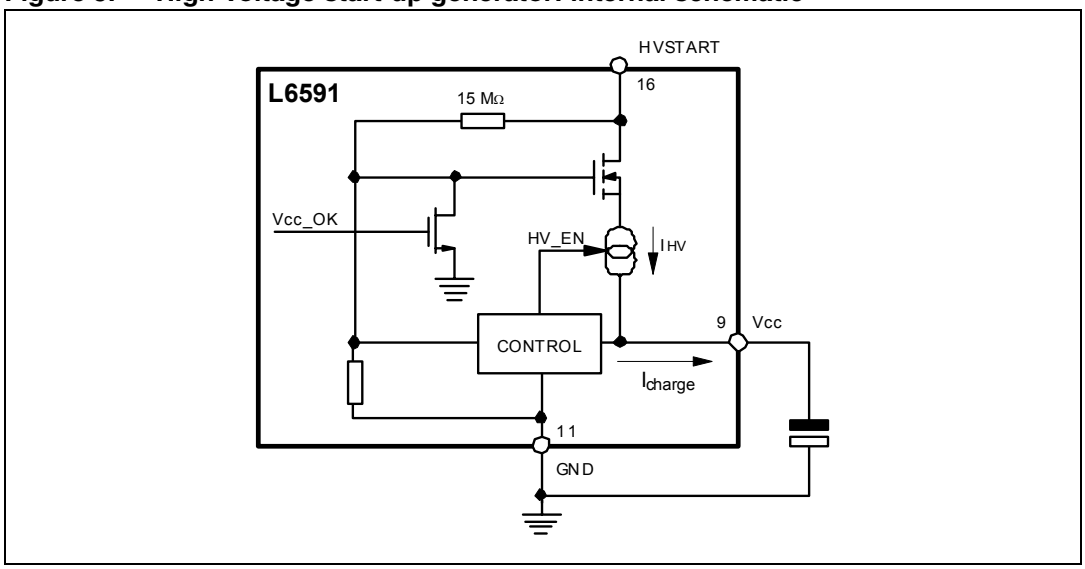
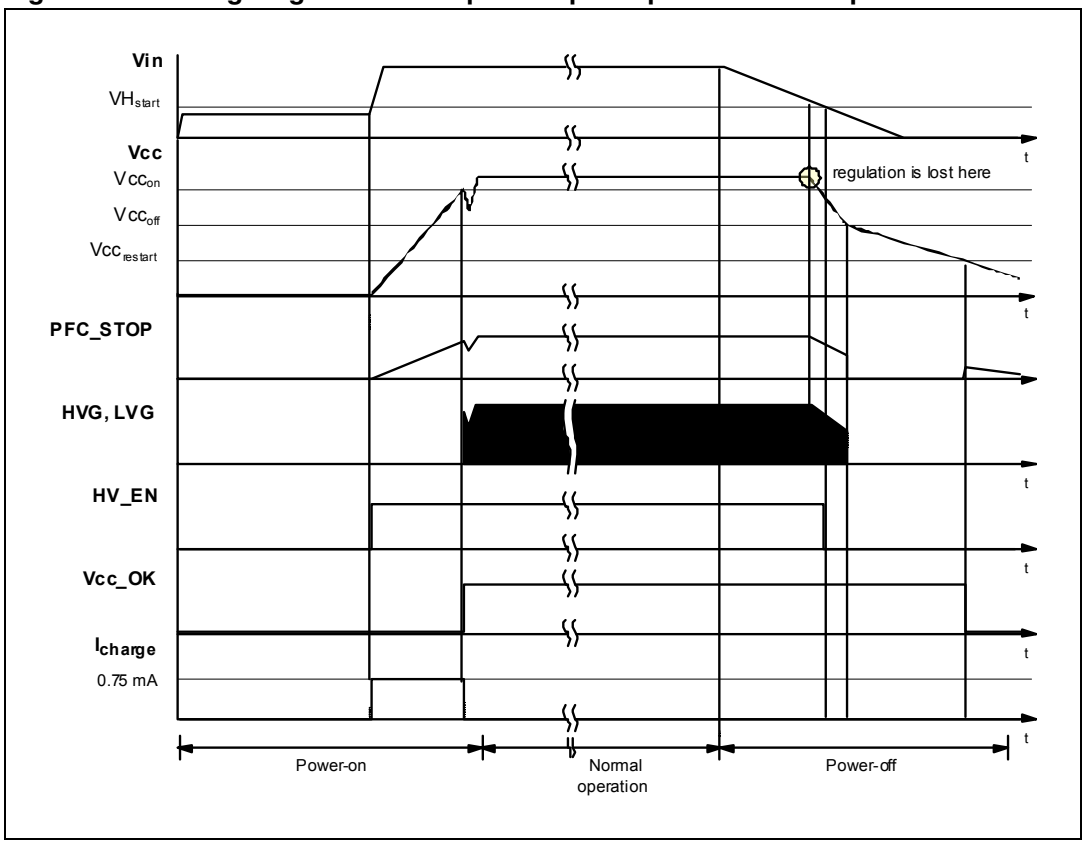


Figure 6. Timing diagram: normal power-up and power-down sequences

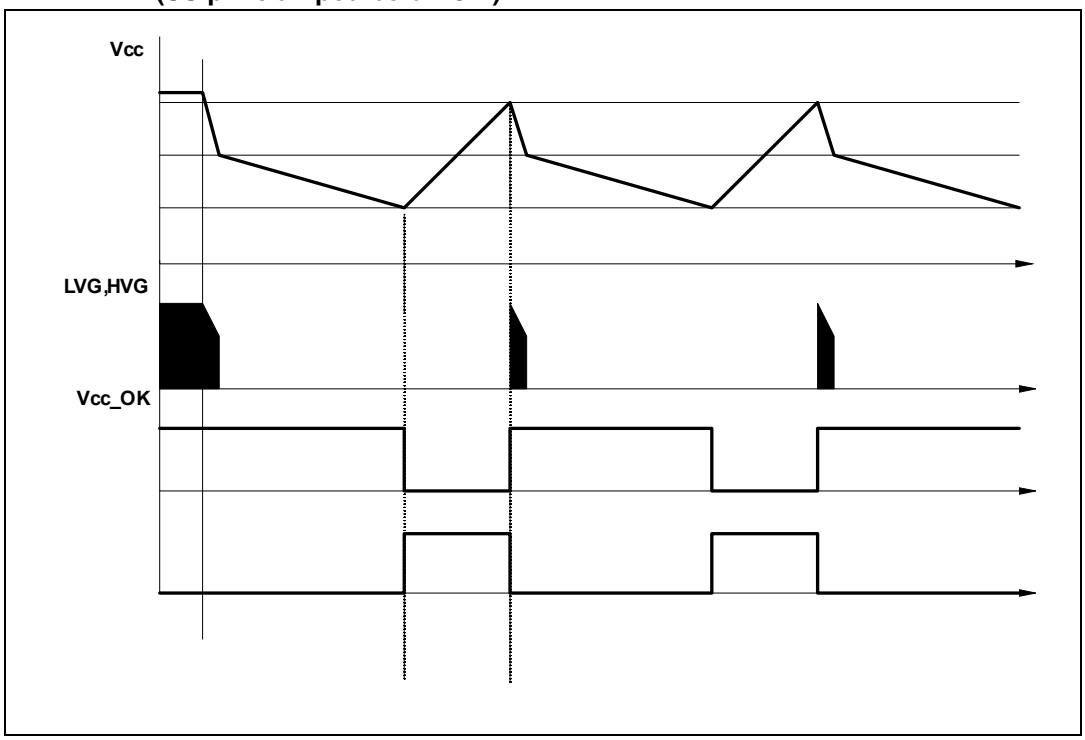


At converter power-down the system will lose regulation as soon as the input voltage is so low that either peak current or maximum duty cycle limitation is tripped. Vcc will then drop and stop IC's activity as it falls below the UVLO threshold (10.5 V typ.). The Vcc_OK signal is de-asserted as the Vcc voltage goes below a threshold Vcc_{rest} located at about 5 V. The HV generator can now restart but, if Vin < Vin_{start}, as shown in *Figure 6*, HV_EN is de-asserted too and the HV generator is disabled. This prevents converter's restart attempts and ensures monotonic output voltage decay at power-down.

The low restart threshold Vcc_{rest} ensures that, during short circuits, the restart attempts of the L6591 will have a very low repetition rate, as shown in the timing diagram of *Figure 7*, and that the converter will work safely with extremely low power throughput.

The restart threshold of the HV generator is changed when any latched disable function of the IC is invoked to ensure a real latch-off. For more details see "*Latched shutdown*" section.

Figure 7. Timing diagram showing short-circuit behavior (SS pin clamped below 5 V)



5.2 Operation at no load or very light load

When the PWM control voltage at pin COMP falls below a threshold located at 1.75 V, the IC is disabled with both the high-side and the low-side MOSFET kept in OFF-state, the oscillator stopped and the quiescent consumption very much reduced to minimize Vcc capacitor discharge.

The control voltage now will increase as a result of the feedback reaction to the energy delivery stop and, as it exceeds 1.82 V, the IC will restart switching. After a while, the control voltage will go down again in response to the energy burst and stop the IC. In this way the converter will work in a burst-mode fashion with a nearly constant peak current. A further load decrease will then cause a frequency reduction, which can go down even to few hundred hertz, thus minimizing all frequency-related losses and making it easier to comply with energy saving regulations. The timing diagram of *Figure 8* illustrates this kind of operation, showing the most significant signals.

If it is necessary to decrease the intervention threshold of the burst-mode operation, this can be done by adding a small DC offset on the current sense pin as shown in *Figure 9.*

Note: The offset reduces the available dynamics of the current signal; thereby, the value of the sense resistor must be determined taking this offset into account.

Figure 8. Load-dependent operating modes: timing diagram

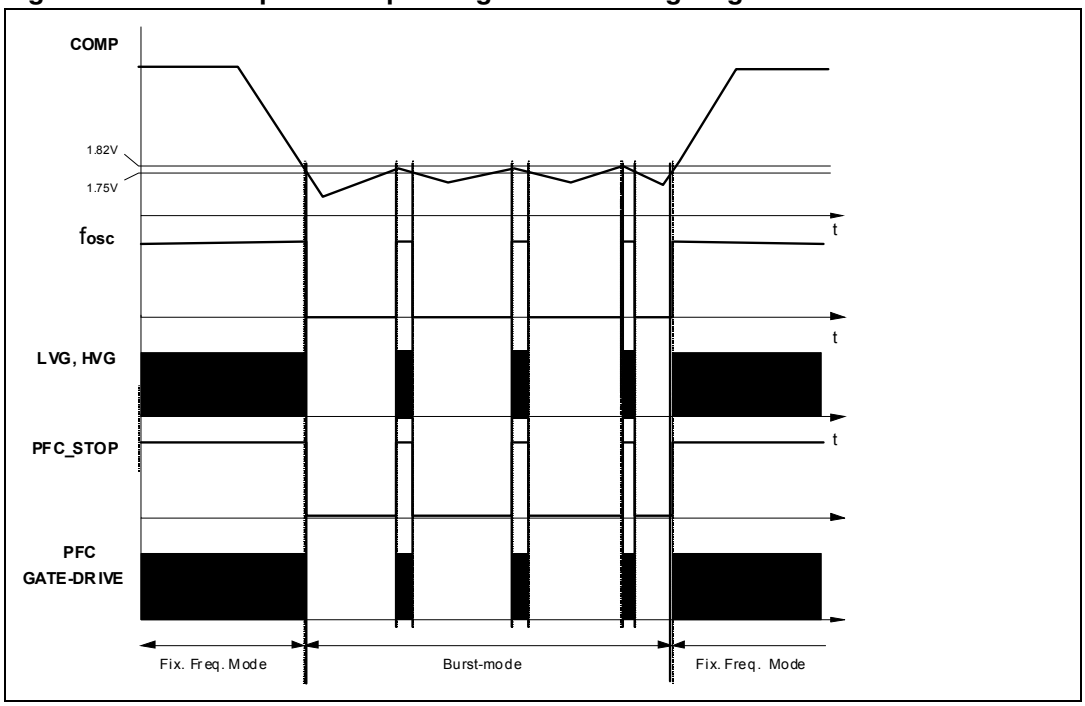
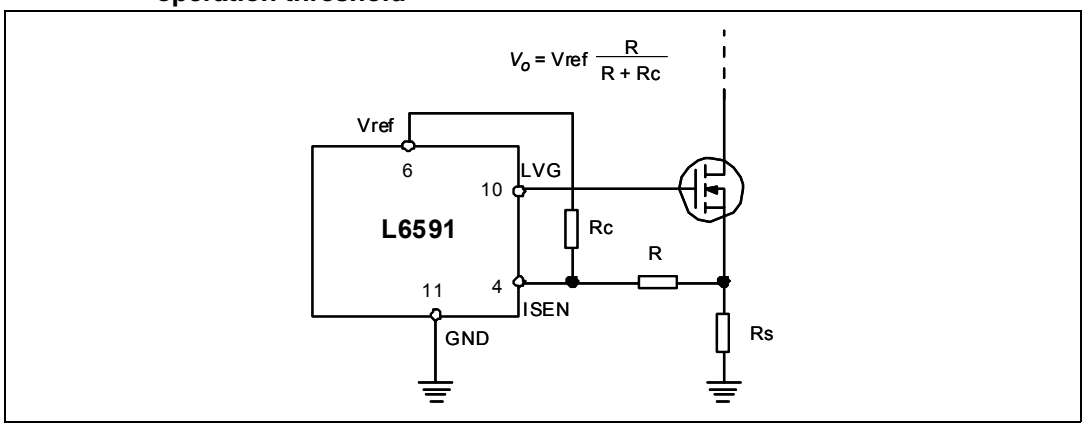


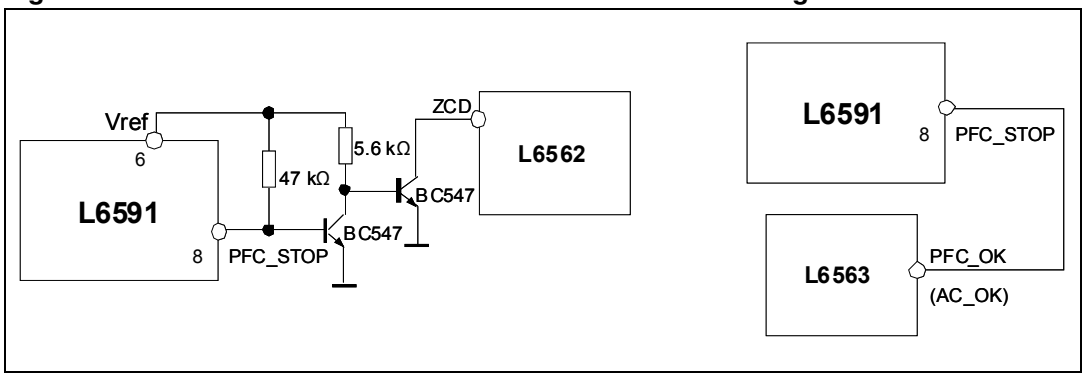
Figure 9. Addition of an offset to the current sense lowers the burst-mode operation threshold



To help the designer meet energy saving requirements even in power-factor-corrected systems, where a PFC pre-regulator precedes the DC-DC converter, the L6591 allows that the PFC pre-regulator can be turned off during burst-mode operation, hence eliminating the no-load consumption of this stage (0.5÷1 W). There is no compliance issue in that because EMC regulations on low-frequency harmonic emissions refer to nominal load, no limit is envisaged when the converter operates with light or no load.

To do so, the L6591 provides the PFC_STOP (#8) pin: it is an open collector output, normally open, that is asserted low when the IC is idle during burst-mode operation. This signal will be externally used for switching off the PFC controller and the pre-regulator as shown in *Figure 10*. When the L6591 is in UVLO the pin is kept open, to let the PFC controller starts first.

Figure 10. How the L6591 can switch off a PFC controller at light load



5.3 PWM control block

The device is specific for secondary feedback. Typically, there is a TL431 at the secondary side and an optocoupler that transfers output voltage information to the PWM control at the primary side, crossing the isolation barrier. The PWM control input (pin #7, COMP) is driven directly by the phototransistor's collector (the emitter is grounded) to modulate the duty cycle. It is recommended to place a small filter capacitor between the pin and GND (#11), as close to the IC as possible to reduce switching noise pick up, to set a pole in the output-to-control transfer function.

5.4 PWM comparator, PWM latch and hiccup-mode OCP

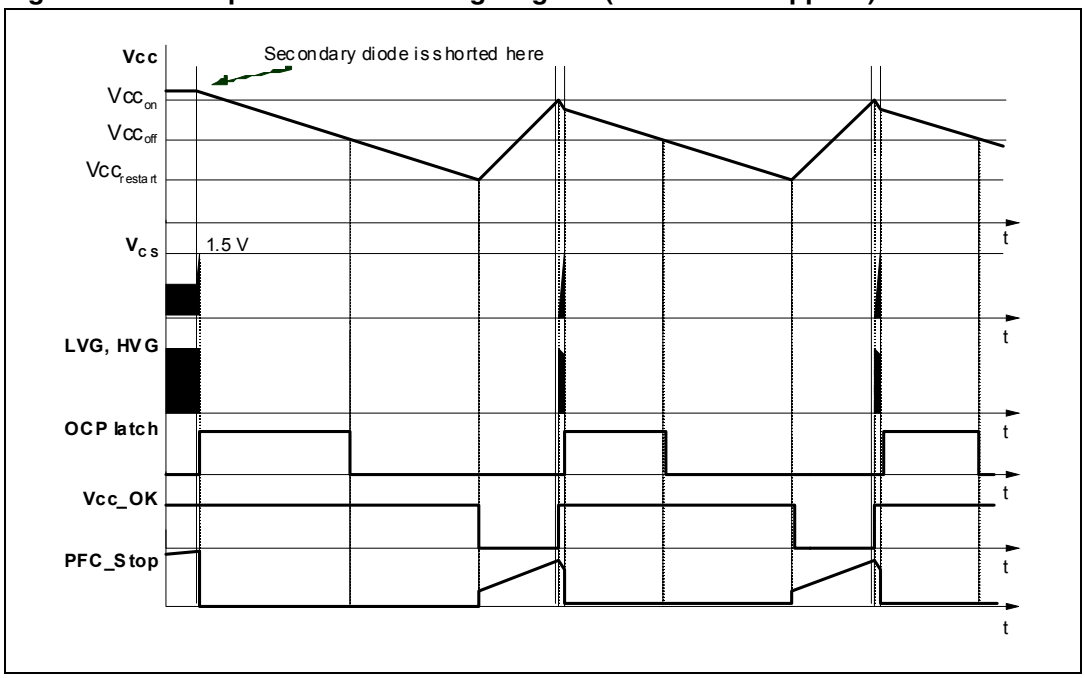
The PWM comparator senses the voltage across the current sense resistor (Rs) and, by comparing it with the programming signal derived by the voltage on pin COMP (#7), determines the exact time when the high-side MOSFET is to be switched off. The PWM latch avoids spurious switching, which might be caused by the noise generated ("double-pulse suppression").

A second comparator senses the voltage on the current sense input and shuts the IC down if the voltage at the pin exceeds 1.5 V. Such an anomalous condition is typically generated by either a short circuit of one of the secondary rectifiers or a shorted secondary winding or a saturated transformer. This condition is latched as long as the IC is supplied; hence if the IC is supplied by an external source it is necessary to disconnect the source to restart the IC.

To distinguish an actual malfunction from a disturbance (e.g. induced during ESD tests), the first time the comparator is tripped the protection circuit enters a "warning state". If in the next switching cycle the comparator is not tripped, a temporary disturbance is assumed and the protection logic will be reset in its idle state; if the comparator will be tripped again a real malfunction is assumed and the L6591 will be stopped.

If the device is self-supplied no energy is coming from the self-supply circuit, then the voltage on the Vcc capacitor will decay and cross the UVLO threshold after some time, which clears the latch. The internal start-up generator is still off, then the Vcc voltage still needs to go below its restart voltage before the Vcc capacitor is charged again and the IC restarted. Ultimately, either of the above mentioned failures will result in a low-frequency intermittent operation (Hiccup-mode operation), with very low stress on the power circuit. The timing diagram of *Figure 11* illustrates this operation.

Figure 11. Hiccup-mode OCP: timing diagram (device self-supplied)

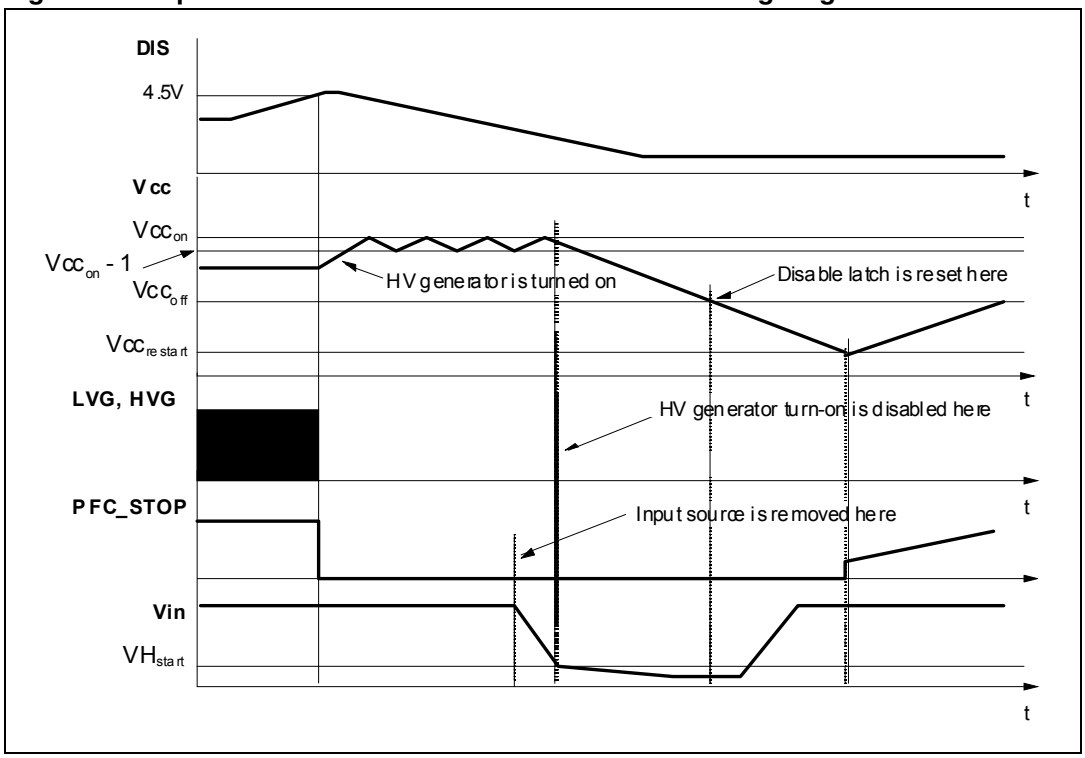


5.5 Latched shutdown

The L6591 is equipped with a comparator having the non-inverting input externally available at the pin DIS (#2) and with the inverting input internally referenced to 4.5 V. As the voltage on the pin exceeds the internal threshold, the IC is immediately shut down and its consumption reduced at a low value.

The information is latched and it is necessary to let the voltage on the Vcc pin go below the UVLO threshold to reset the latch and restart the IC. To keep the latch supplied as long as the converter is connected to the input source, the HV generator is activated periodically so that Vcc oscillates between the start-up threshold V_{ccON} and V_{ccON} – 1 V. It is then necessary to disconnect the converter from the input source to restart the IC. This operation is shown in the timing diagram of *Figure 12*. Activating the HV generator in this way cuts its power dissipation approximately by three (as compared to the case of continuous conduction) and keeps peak silicon temperature close to the average value.

Figure 12. Operation after latched disable activation: timing diagram



This function is useful to implement a latched over temperature protection very easily by biasing the pin with a divider from VREF, where the upper resistor is an NTC physically located close to a heating element like the MOSFET, or the secondary diode or the transformer. An OVP can be implemented as well, e.g. by sensing the output voltage and transferring an overvoltage condition via an optocoupler.

5.6 Oscillator and dead-time programming

The oscillator is programmed externally by means of a resistor-capacitor network (R_T, C_T) connected from pin OSC (#5) to VREF (#6) and to ground respectively. Once chosen the oscillator frequency and the dead-time duration needed, the values of RT and CT can be calculated as:

Equation 1

$$R_T = 50 + \frac{1150}{f_{osc}\left(T_d - 125 \cdot 10^{-9}\right)}$$

Equation 2

$$C_T = 1.39 \cdot \frac{1}{f_{osc}} \cdot \frac{R_T - 1200}{R_T\left(R_T - 50\right)}$$

After having selected the commercial values for R_T and C_T, the oscillator frequency (f_{osc}) can be verified with good approximation using the following formula:

Equation 3

$$f_{osc} \approx \frac{1.39}{(C_T (R_T + 1150))}$$

During the negative-going ramp of the sawtooth a clock pulse is released. A T flip-flop, along with a logic circuit, separates the odd and the even clock pulses. The even ones turn off the low-side MOSFET first and, after a dead time T_d, turn on the high-side MOSFET. Normally, the high-side MOSFET is turned off (and the low-side MOSFET turned on after the dead time T_d) in response to the control loop; in case of overload it will be the overcurrent comparator to do the job or, in case of open control loop, the odd clock pulses will limit the maximum ON-time within one oscillator cycle. In this way, the maximum duty cycle will be limited right below 50 % and the operating frequency of the converter will be half that of the oscillator. Precisely, with reference to the waveforms in *Figure 15*, where $T_{sw} = 2/f_{osc}$, the maximum achievable duty cycle is:

Equation 4

$$D_{max} = \frac{\frac{T_{SW}}{2} - T_d}{T_{SW}} = 0.5 - \frac{T_d}{T_{SW}} = 0.5\left(1 - T_d f_{osc}\right)$$

At start-up the first clock pulse will turn on the low-side MOSFET for 10 oscillator cycles to charge the bootstrap capacitor and then the high-side MOSFET will switch on. When the IC resumes switching during burst-mode operation the first clock pulse will turn-on the low-side MOSFET first to charge the bootstrap capacitor, and just after the second clock pulse the high-side MOSFET will switch-on. In this way the bootstrap capacitor will always be charged and ready to supply the high-side floating driver. The oscillator waveforms are illustrated in *Figure 15* as well.

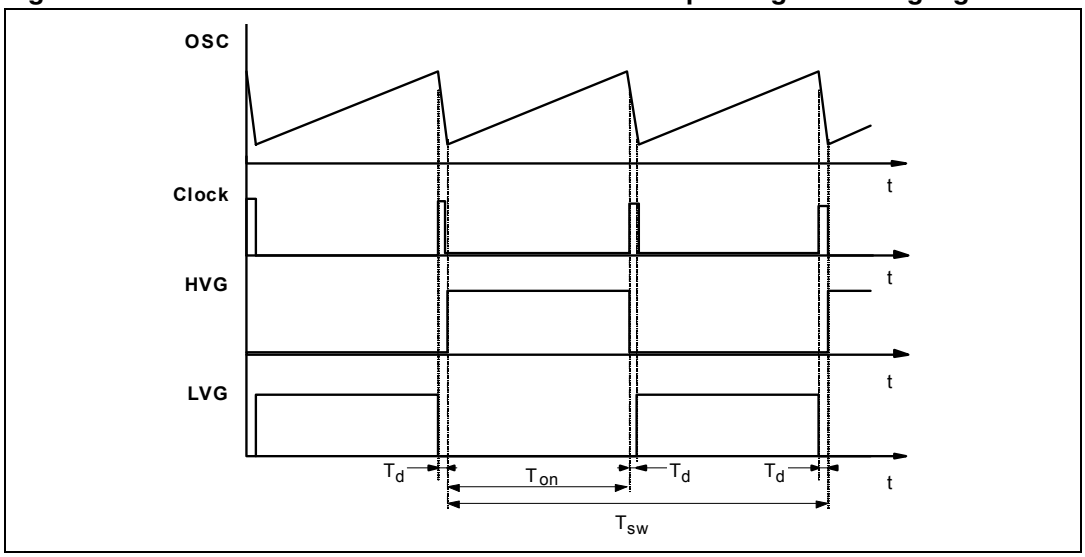
The dead-time T_d equals the duration of the negative-going ramp of the oscillator sawtooth plus an internal delay of 125 ns; hence it depends on the timing capacitor C_T and the resistor R_T and is given by the approximate relationship:

Equation 5

$$T_d = C_T \frac{2.1}{2.54 \cdot 10^{-3} - \frac{3.05}{R_T}} + 125 \cdot 10^{-9}$$

There is an internal 325 ns limit to the minimum T_d value, to make sure that no hazardous condition of shoot-through can be generated, however it is recommended not to use capacitor values lower than 220 pF.

Figure 13. Oscillator waveforms and their relationship with gate-driving signals

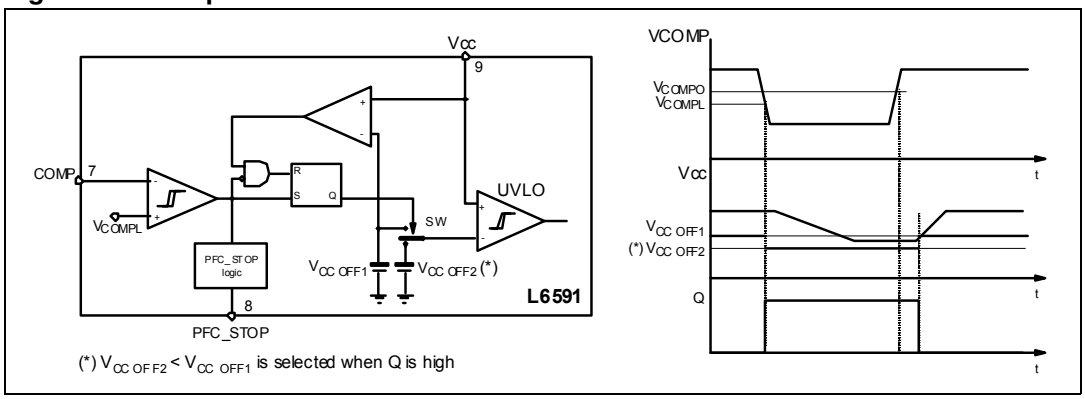


5.7 Adaptive UVLO

A major problem when optimizing a converter for minimum no-load consumption is that the voltage generated by the self-supply system under these conditions falls considerably as compared even to a few mA load. This very often causes the IC's supply voltage Vcc to drop and go below the UVLO threshold of the controller so that the operation becomes intermittent, which is undesired. A low UVLO threshold would be helpful but it could be an issue to drive the MOSFETS with a sufficient gate-drive voltage at heavy load during power off.

To help the designer overcome this problem, the L6591, besides reducing its own consumption during burst-mode operation, also features a proprietary adaptive UVLO function. It consists of shifting the UVLO threshold downwards at light load, namely when the voltage at pin COMP falls below a threshold V_{COMPL} internally fixed, so as to provide more headroom. To prevent any malfunctioning during transients from minimum to maximum load the normal (higher) UVLO threshold is re-established when the voltage at pin COMP exceeds V_{COMPL} (with some mV hysteresis) and Vcc has exceeded the normal UVLO threshold (see *Figure 16*). The normal UVLO threshold ensures that under heavy load conditions the MOSFETS will be driven with an appropriate gate voltage.

Figure 14. Adaptive UVLO block

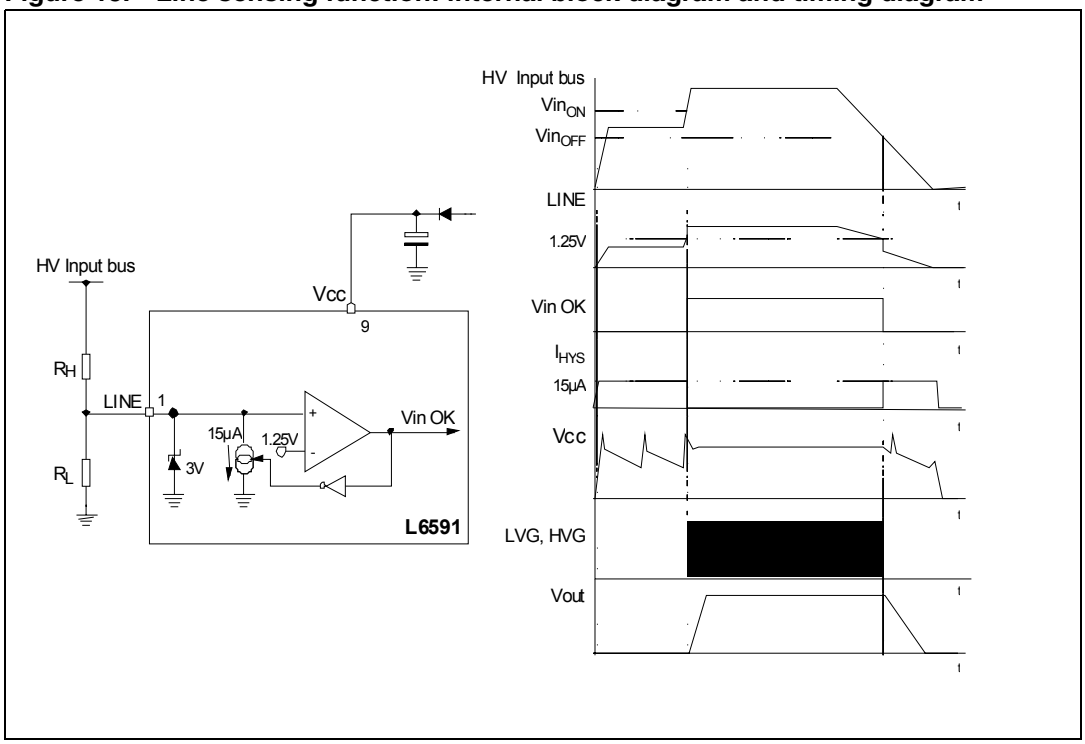


5.8 Line sensing function

This function basically stops the IC as the input voltage to the converter falls below the specified range and lets it restart as the voltage goes back within the range. The sensed voltage can be either the rectified and filtered mains voltage, in which case the function will act as a brownout protection, or, in systems with a PFC pre-regulator front-end, the output voltage of the PFC stage, in which case the function will serve as a power-on and power-off sequencing.

L6591 shutdown upon input under voltage is accomplished by means of an internal comparator, as shown in the block diagram of *Figure 17*, whose non-inverting input is available at the LINE pin (#1). The comparator is internally referenced to 1.25 V and disables the IC if the voltage applied at the LINE pin is below the internal reference. Under these conditions the soft-start discharged, the pin PFC_STOP is open and the consumption of the IC is reduced. PWM operation is re-enabled as the voltage on the pin is above the reference. The comparator is provided with current hysteresis instead of a more usual voltage hysteresis: an internal 15 µA current sink is ON as long as the voltage applied at the LINE pin is below the reference and is OFF if the voltage is above the reference.

Figure 15. Line sensing function: internal block diagram and timing diagram



This approach provides an additional degree of freedom: it is possible to set the ON threshold and the OFF threshold separately by properly choosing the resistors of the external divider (see below). With voltage hysteresis, instead, fixing one threshold automatically fixes the other one depending on the built-in hysteresis of the comparator.

With reference to *Figure 17*, the following relationships can be established for the ON (V_{inON}) and OFF (V_{inOFF}) thresholds of the input voltage:

Equation 6

$$\frac{Vin_{ON} - 1.25}{R_H} = 15 \cdot 10^{-6} + \frac{1.25}{R_L} \qquad \frac{Vin_{OFF} - 1.25}{R_H} = \frac{1.25}{R_L}$$

Which, solved for R_H and R_L, yield:

Equation 7

$$R_H = \frac{Vin_{ON} - Vin_{OFF}}{15 \cdot 10^{-6}}; \qquad R_L = R_H \frac{1.25}{Vin_{OFF} - 1.25}$$

While the line undervoltage is active the start-up generator keeps on working but there is no PWM activity, thus the Vcc voltage continuously oscillates between the start-up and the UVLO thresholds, as shown in the timing diagram of *Figure 17*.

The LINE pin, while the device is operating, is a high impedance input connected to high value resistors, thus it is prone to pick up noise, which might alter the OFF threshold or give origin to undesired switch-off of the IC during ESD tests. It is possible to bypass the pin to ground with a small film capacitor (e.g. 1-10 nF) to prevent any malfunctioning of this kind. If the function is not used the pin has to be connected to the VREF pin (#6) through a resistor in the range of 10 to 100 kΩ.

5.9 Soft-start and delayed latched shutdown upon overcurrent

At device start-up, a capacitor (Css) connected between the SS pin (#4) and ground is charged by an internal current generator, I_{SS1}, from zero up to about 2 V where it is clamped. During this ramp, the overcurrent setpoint progressively raises from zero the final value (0.8 V). The time needed for the overcurrent setpoint to reach its steady state value, referred to as soft-start time, is approximately:

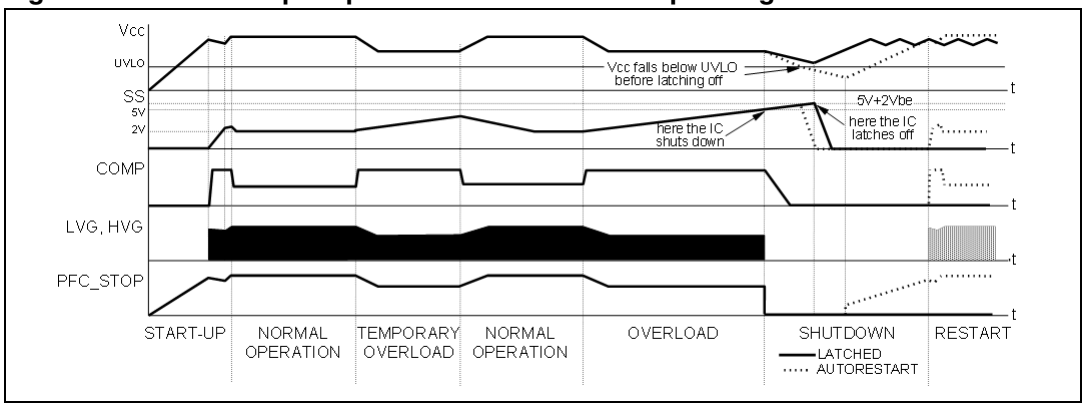
Equation 8

$$T_{SS} = 0.8 \frac{C_{SS}}{I_{SS1}}$$

During the ramp, the MOSFET duty cycle increases progressively, hence controlling the start-up inrush current. Furthermore, all the functions that monitor the voltage on pin COMP are disabled.

The soft-start pin is also invoked whenever the control voltage (COMP) saturates high, which reveals an open-loop condition for the feedback system. This condition very often occurs at start-up, but may be also caused by either a control loop failure or a converter overload/short circuit.

Figure 16. Soft-start pin operation under different operating conditions



While in case of feedback loop failure the system must be stopped quickly to prevent the output voltage from reaching too high values, an overload or a short circuit does not generally need such fast intervention. The L6591 makes it easier to handle such conditions: the 2 V clamp on the SS pin is removed and a second internal current generator $I_{SS2} = I_{SS1}/4$ keeps on charging Css. If the voltage reaches 5 V the IC will be disabled, if it is allowed to reach 2 V_{BE} over 5 V, the IC will be latched off. In the former case the resulting behavior will be identical to that under short circuit illustrated in *Figure 11*; in the latter case the result will be identical to that of *Figure 12*. The time delay before stopping switching upon overload is:

Equation 9

$$T_{delay} = 12\frac{C_{SS}}{I_{SS1}}$$

If the overload disappears before the SS voltage reaches 5 V the I_{SS2} generator will be turned off and the voltage gradually brought back down to 2 V. A diode, with the anode to the SS pin and the cathode connected to the VREF pin (#6) allows the designer to select either an auto-restart mode or a latch-mode behavior upon overload.

If latch-mode behavior is desired also for converter's short circuit, make sure that the supply voltage of the IC never falls below the UVLO threshold before activating the latch. *Figure 18* shows soft-start pin behavior under different operating conditions.

Figure 17 shows a typical high-power adapter application that uses the L6591 in conjunction with the L6563 PFC controller.

6 Summary of L6591 power management functions

It has been seen that the device is provided with a number of power management functions: different operating mode upon loading conditions, protection functions, as well as interaction with the PFC pre-regulator. To help the designer familiarize with these functions, in the following tables all of theme are summarized with their respective activation mechanism and the resulting status of the most important pins. This can be useful not only for a correct use of the IC but also for diagnostic purposes: especially at prototyping/debugging stage, it is quite common to bump into unwanted activation of some function, and these tables can be used as a sort of quick troubleshooting guide.

Table 5. Light load management

Feature	Description	Caused by	IC behavior	Vcc restart [V]	Consumption [mA]	PFC_STOP	SS	OSC
Burst mode	Controlled ON-OFF operation for low power consumption at light load	$V_{COMP} < V_{COMPBon}$	Pulse skipping operation	N.A.	2 mA max when $V_{COMP} < V_{COMPBon}$	Active (low) when $V_{COMP} < V_{COMPBon}$	No change	Stopped when $V_{COMP} < V_{COMPBon}$
Adaptive UVLO	Extended Vcc range at light load	$V_{COMP} < V_{COMPL}$	UVLO threshold reduction	N.A.	N.A.	No change	No change	Run

Table 6. Protections

Protection	Description	Caused by	IC behavior	Vcc restart [V]	IC Iq [mA]	VREF [V]	SS	V_{COMP} [V]	OSC [V]	PFC_STOP
OLP	Output overload protection	$V_{COMP} = V_{COMPH}$ $V_{SS} > V_{SSDIS}$	Auto restart (1)	5	1.2	5	N.A.	0	Stop	Active (low)
		$V_{COMP} = V_{COMPH}$ $V_{SS} > V_{SSLAT}$	Latched	13	0.35 max	0	N.A.	0	Stop	Active (low)
Short circuit protection	Output short circuit protection	$V_{COMP} = V_{COMPH}$ $V_{SS} > V_{SSDIS}$	Auto restart (1)	5	1.2	5	N.A.	0	Stop	Active (low)
		$V_{COMP} = V_{COMPH}$ $V_{SS} > V_{SSLAT}$	Latched	13	0.35 max	0	N.A.	0	Stop	Active (low)

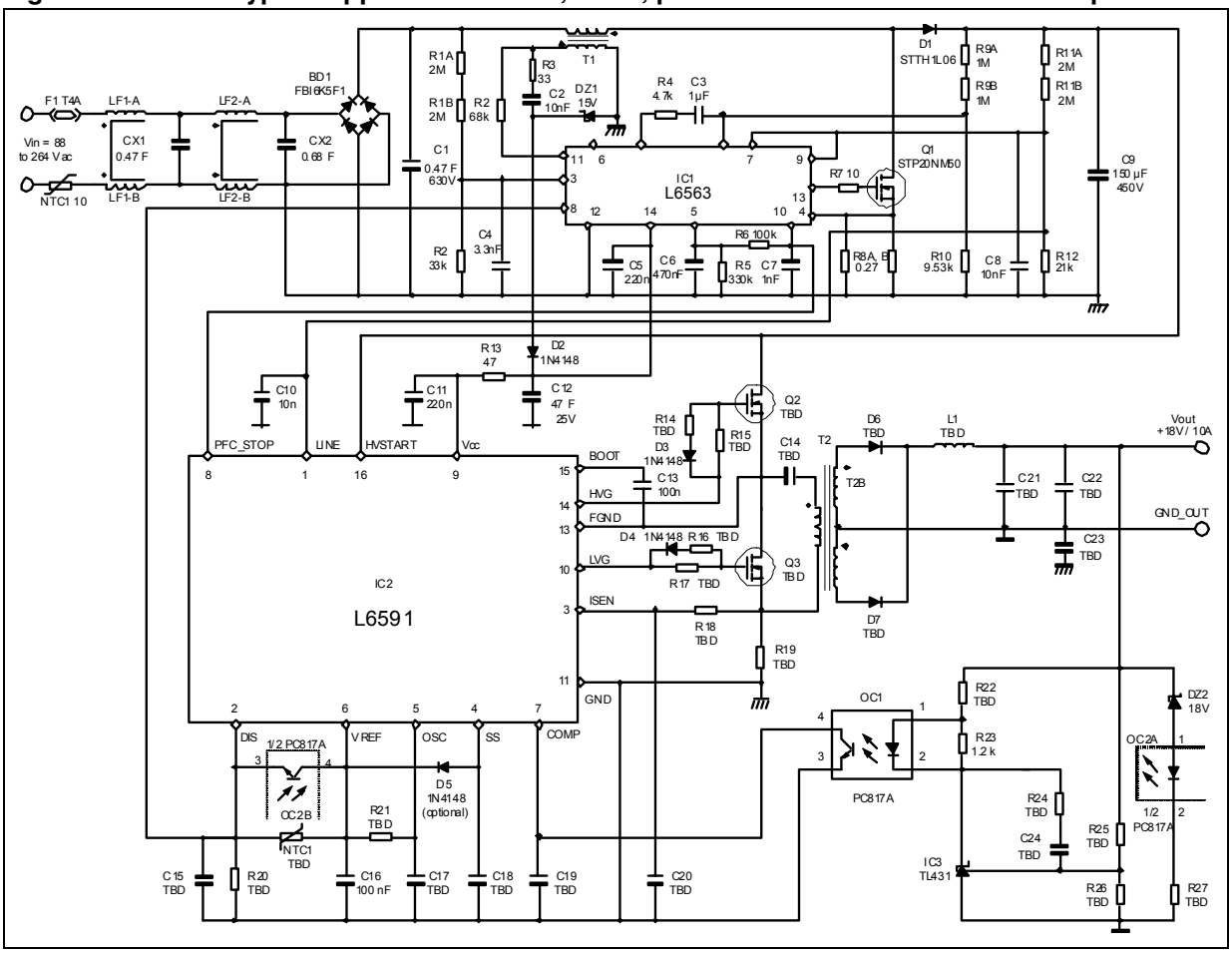
Table 6. Protections (continued)

Protection	Description	Caused by	IC behavior	Vcc restart [V]	IC Iq [mA]	VREF [V]	SS	V_{COMP} [V]	OSC [V]	PFC_STOP
2nd OCP	Transformer saturation or shorted secondary diode protection	V_{ISEN} > 1.5 V for 2 consecutive switching cycles	Latched (2)	5	0.35 max	0	0	0	Stop	Active (low)
DISABLE	Externally programmable latched protection	V_{DIS} > 4.5 V	Latched	13	0.35 max	0	0	0	Stop	Active (low)
Brownout	Mains undervoltage protection	V_{LINE} < 1.25 V	Auto restart	5	0.35 max	0	0	0	Stop	Not active (high Z)

1. Use one external diode from SS (#14) to VREF (#10), cathode to VREF.
2. The condition is latched as long as the IC is supplied; the HV generator is not invoked.
3. All values are typical unless otherwise specified.

It is worth reminding that “auto-restart” means that the device will work intermittently as long as the condition that is activating the function is not removed; “Latched” means that the device is stopped as long as the unit is connected to the input power source and the unit must be disconnected for some time from the source in order for the device (and the unit) to restart.

Figure 17. L6591 typical application: 180 W, WRM, power-factor-corrected AC-DC adapter



7 Package mechanical data

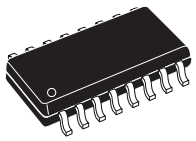
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 18. SO16N package dimensions

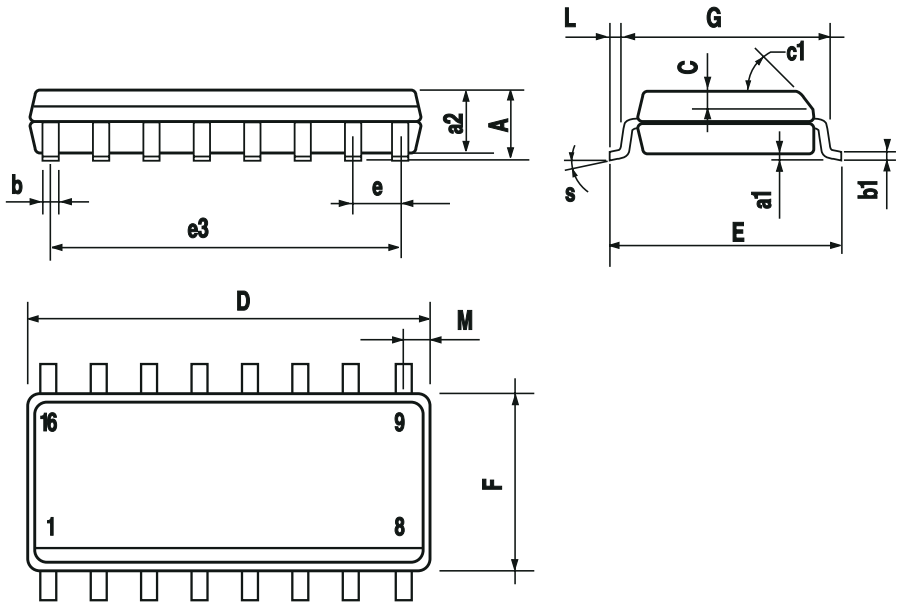
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.009
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1			45°	(typ.)		
D(1)	9.8		10	0.386		0.394
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F(1)	3.8		4.0	0.150		0.157
G	4.60		5.30	0.181		0.208
L	0.4		1.27	0.150		0.050
M			0.62			0.024
S	8 ° (max.)					

(1) "D" and "F" do not include mold flash or protrusions - Mold flash or protrusions shall not exceed 0.15mm (.006inc.)

OUTLINE AND MECHANICAL DATA



SO16N



8 Order codes

Table 7. Order codes

Order codes	Package	Packaging
L6591	SO16N	Tube
L6591TR	SO16N	Tape and reel

9 Revision history

Table 8. Document revision history

Date	Revision	Changes
19-Jun-2008	1	Initial release

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